

Abstract

A high-speed parallel data communication approach overcomes data skewing concerns by concurrently transmitting data in a plurality of multiple-bit groups and, after receiving the concurrently-transmitted data, realigning skew-caused misalignments between the groups. In one particular example embodiment, for each group, an arrangement transfers the data in parallel and along with a clock signal for synchronizing digital data. The transferred digital data is synchronously collected via the clock signal for the group. At the receiving module, the data collected for each group is aligned using each group's dedicated clock signal. Skew across clock-domain groups is tolerated and overcome by processing the data and the skew first within each clock domain group, and then between groups.